SIGMA DELTA MODULATED PHASE LOCK LOOP WITH PHASE INTERPOLATION TEO ET. AL

MP0359 /CUST. NO.: 23624 SHEET 1/6

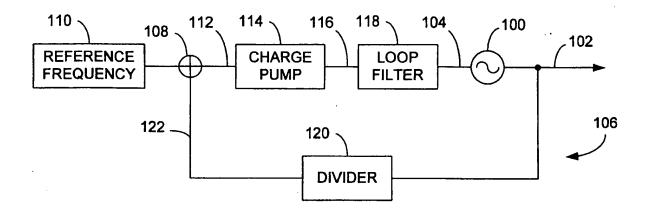


FIG. 1 (Prior Art)

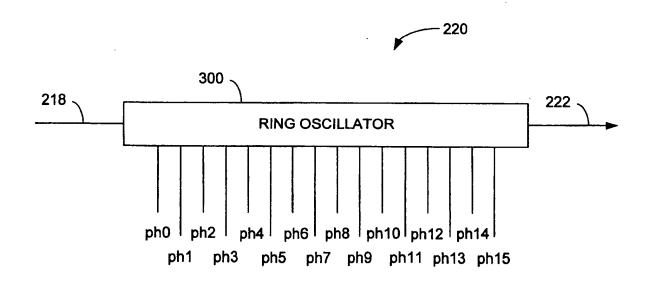
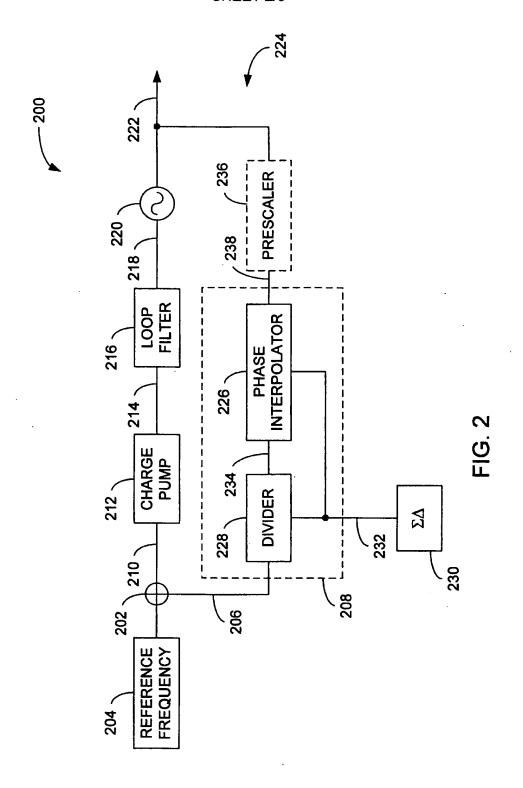


FIG. 3

SIGMA DELTA MODULATED PHASE LOCK LOOP WITH PHASE INTERPOLATION

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SIGMA DELTA MODULATED PHASE LOCK LOOP WITH PHASE INTERPOLATION

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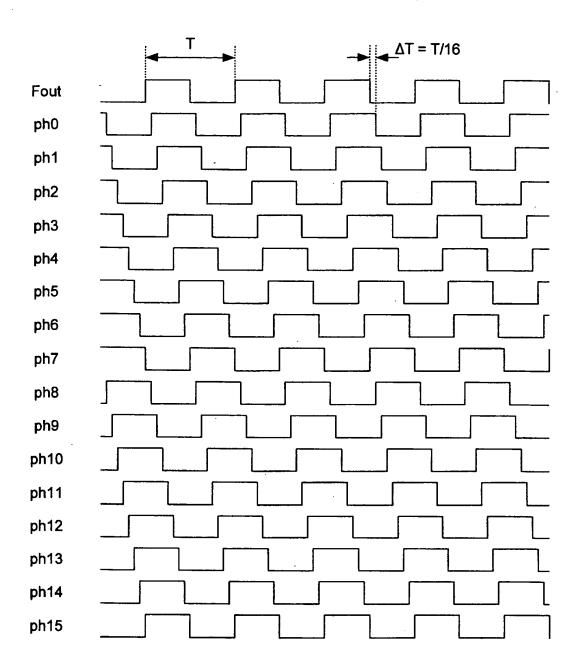
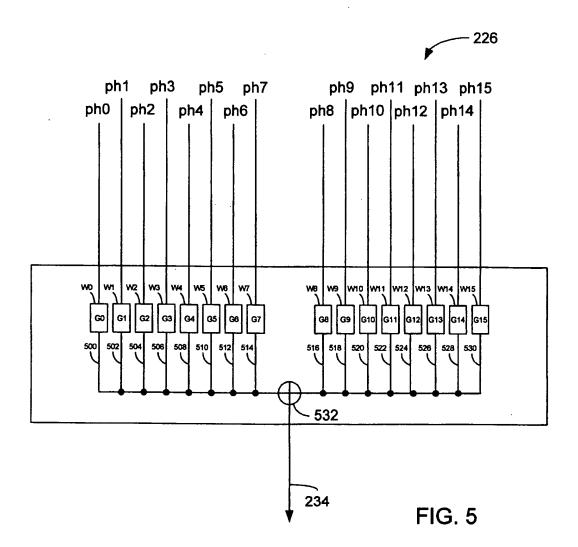


FIG. 4

SIGMA DELTA MODULATED PHASE LOCK LOOP WITH PHASE INTERPOLATION

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SIGMA DELTA MODULATED PHASE LOCK LOOP WITH PHASE INTERPOLATION TEO ET. AL MP0359 /CUST. NO.: 23624 600 SHEET 5/6 602 GENERATE AN OUTPUT HAVING A CONTROLLABLE FREQUENCY 604 GENERATE ONE OR MORE SIGNALS DELAYED WITH RESPECT TO THE OUTPUT 606 INTERPOLATE THE DELAYED SIGNALS BASED IN PART ON A CONTROL SIGNAL RECEIVED FROM A ΣΔ MODULATOR TO GENERATE AN INTERPOLATED OUTPUT **SIGNAL** 608 DIVIDE THE INTERPOLATED OUTPUT (e.g., USING A FRACTIONAL N DIVIDER) TO GENERATE A DIVIDED OUTPUT **SIGNAL** 610 COMPARE THE DIVIDED OUTPUT TO A FIXED REFERENCE SIGNAL TO **GENERATE AN ERROR SIGNAL** 612 ADJUST THE OUTPUT BASED ON THE ERROR SIGNAL

FIG. 6

SIGMA DELTA MODULATED PHASE LOCK LOOP WITH PHASE INTERPOLATION TEO ET. AL

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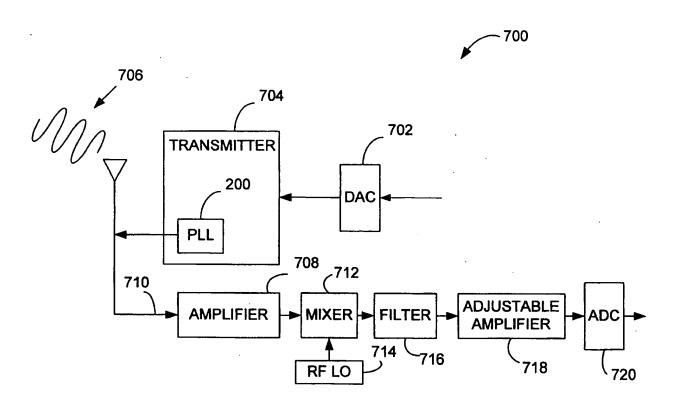


FIG. 7